REMARKS

I. Summary of Office Action

Claims 1-34 are pending in the above-identified application.

The Examiner objected to the abstract of the invention because it contains the undefined acronym DSP.

The Examiner rejected claims 7-10, 18-21 and 26-34 under 35 U.S.C. § 112, second paragraph, as being indefinite because the terms "analysis logic" and "analysis circuit" are allegedly not understood.

The Examiner rejected claims 1-3 and 11-17 under 35 U.S.C. § 102(e) as being anticipated by Fandrianto et al. U.S. patent No. 6,441,842 (hereinafter "Fandrianto"). The Examiner rejected claims 1-3, 11-12 and 14-17 under 35 U.S.C. § 102(e) as being anticipated by Duncan et al. U.S. patent No. 6,597,394 (hereinafter "Duncan"). The Examiner also rejected claims 1-3, 11-12 and 14-17 under 35 U.S.C. § 102(e) as being anticipated by Thi et al U.S. patent publication No. US 2002/0061012 (hereinafter "Thi").

The Examiner rejected claims 22-27 and 31-34 under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi. The Examiner rejected claim 4

under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi in view of Lim et al. U.S. patent No. 6,209,017 (hereinafter "Lim"). The Examiner rejected claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi in view of Lim and in further view of Nguyen et al. 6,519,620 (hereinafter "Nguyen").

The Examiner objected to claims 7-10, 18-21 and 28-30 for depending from rejected independent claims 1, 11 and 26. The Examiner stated they would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

II. Summary of Applicant's Reply to Office Action

The specification has been amended to overcome the Examiner's objection to the abstract. Applicant notes with appreciation the indication of allowable subject matter in claims 7-10, 18-21 and 28-30. Claims 7-10, 18-21 and 28-30 have been amended to be written in independent form and include all of the limitations of the base claims and any intervening claims. No new subject matter has been added and the amendments are fully supported by the application as filed. The Examiner's claim rejections are respectfully traversed.

III. Applicant's Reply to the Claim Rejections

A. The 112 Rejection

The Examiner rejected claims 7-10, 18-21 and 26-34 under 35 U.S.C. § 112, second paragraph, as being indefinite because the terms "analysis logic" and "analysis circuit" are allegedly not understood. The Examiner's rejection is respectfully traversed.

Independent claim 1, as well as independent claim 7, which was amended to include all the limitation of claim 1, relate to a method for processing signals on a programmable logic device that includes a plurality of logic regions. At least one of these logic regions is configured as "word conditioning logic". Claim 7, further specifies that at least a further one of these regions is configured as "analysis logic". As can be seen from claims 8-9, which depend from claim 7, analysis logic is logic in which an analysis operation may be performed. As can be seen from claims 4 and 5, which depend from claim 1, the word conditioning logic may include saturation logic that may be used for monitoring signals. Similarly, the analysis logic may be used to perform block floating point analysis, as can

be seen from claim 10, which depends from claim 7. Accordingly, similar to how the term "word conditioning logic" refers to logic in which a word conditioning operation may be performed, the term "analysis logic", as used in claims 7-10, refers to logic in which an analysis operation such as block floating point analysis may be performed. See, e.g., applicant's specification, page 1, lines 9-24, page 4, lines 11-13 and page 7, lines 5-11. Likewise, the term "analysis logic", as used in claims 18-21, refers to logic in which an analysis operation such as block floating point analysis may be performed.

The term "analysis circuit" referred to by the Examiner is part of the term "data conditioning and analysis circuit" in claims 26-34. Independent claim 26, as well as independent claims 28-30, which were amended to include at least all the limitations of claim 26, relate to a programmable logic integrated circuit device that includes a plurality of logic regions. At least one region is configured as a "data conditioning and analysis circuit". Claims 31-34 depend from claim 26. Claim 27, which depends from claim 26, further specifies that the data conditioning and analysis circuit comprises at least one *word*

conditioning subcircuit and at least one *analysis* subcircuit. As discussed above and as can be seen from applicant's specification, an example of an *analysis* operation is a block floating point analysis, while an example of a *word conditioning* operation is signal monitoring for saturation. *Supra.* Accordingly, the term "data conditioning and analysis circuit", as used in claims 26-34, refers to a circuit that may perform an analysis operation such as block floating point analysis, and a word conditioning operation such as signal monitoring for saturation.

Applicant respectfully requests that the rejection of claims 7-10, 18-21 and 26-34 under 35 U.S.C. § 112, second paragraph, be withdrawn.

B. The 102 Rejections

The Examiner rejected claims 1-3 and 11-17 under 35 U.S.C. § 102(e) as being anticipated by Fandrianto. The Examiner rejected claims 1-3, 11-12 and 14-17 under 35 U.S.C. § 102(e) as being anticipated by Duncan. The Examiner also rejected claims 1-3, 11-12 and 14-17 under 35 U.S.C. § 102(e) as being anticipated by Thi. The Examiner's rejections are respectfully traversed.

Independent claims 1 and 11 are directed towards systems and methods that relate to a programmable logic device having at least one region configured as a computation unit (e.g., a multiplier-accumulator (MAC) block) and at least another region configured as word conditioning logic (e.g., logic for performing saturation operations). The computation unit is configured to propagate signals received on its input to its output via a critical path without propagating the signals through the word conditioning logic. A datapath propagates output signals from the computation unit to a storage destination (e.g., a memory structure) through the word conditioning logic. By shifting the propagation delay associated with the word conditioning logic from the critical path to a separate datapath (e.g., a write datapath), system throughput is improved.

Fandrianto relates to a cost-effective video communication system that utilizes a video compression/decompression processing scheme for communicating video data over a telephone line. The video communication system includes a programmable processor circuit that includes a data-flow path having an integrated

arrangement of discrete circuits including MACs. Each MAC has a programmable clamp that allows clamping to essentially any precision. Abstract, column 2, lines 51-65, column 21, lines 13-46 and FIG. 13.

Duncan relates to a programmable image transform processor having a programmable arithmetic block that can perform MAC functions and that can be configured to perform saturation and rounding operations. Abstract, column 14, line 66 through column 15, line 15, column 17, lines 35-51 and FIG. 6A.

Thi relates to a system for interfacing telephony devices with a Data Over Cable Service Interface Specification compatible networks. The system includes an audio co-processor having a programmable MAC data path that includes a store block that can perform MAC functions as well as rounding and saturation operations. Paragraphs 0002 and 0306, and FIG. 34.

The Examiner contends that each of Fandrianto, Duncan and Thi discloses all the features of applicant's independent claims 1 and 11. Applicant respectfully disagrees.

Although Fandrianto, Duncan and Thi arguably disclose computation units and word conditioning logic, these components are disposed along a single datapath where the word conditioning functionality is incorporated into the computation unit. See Fandrianto, FIG. 13 (clamp 626 is part of MAC 148.3), Duncan, column 17, lines 49-51 (description of block 450) and Thi, paragraph 0306 (description of block 4026). Applicant's claimed invention specifically teaches away from doing so and therefore achieves better system performance.

Applicant's claimed invention eliminates the propagation delay incurred as a result of passing through word conditioning logic from the critical path of a computation unit. By shifting the propagation delay associated with the word conditioning logic from the critical path to a separate datapath, system throughput is improved. See, e.g., applicant's specification, page 5, line 22 through page 6, line 6.

Unlike applicant's claimed invention, none of the references that are relied on by the Examiner show or suggest providing a separate datapath from the output of the computation unit to a storage destination, where signals on

the datapath are propagated through word conditioning logic, in addition to a critical path through which signals are propagated from the input of the computation unit to its output without propagating through the word conditioning logic, as specified in claims 1 and 11.

Accordingly, neither Fandrianto, Duncan nor Thi show or suggest all the features of amended independent claims 1 and 11. Applicants therefore respectfully submit that independent claims 1 and 11 are allowable. Because claims 2-3 depend from claim 1, and claims 12-17 depend from claim 11, applicant respectfully submits that these claims are also allowable. Applicant respectfully requests that the rejections of claims 1-3 and 11-17 under 35 U.S.C. § 102(e) be withdrawn.

C. The 103 Rejections

The Examiner rejected claims 22-27 and 31-34 under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi. The Examiner rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi in view of Lim. The Examiner

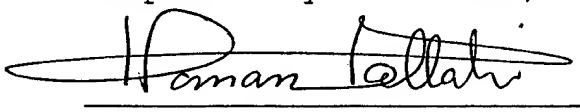
rejected claims 5-6 under 35 U.S.C. § 103(a) as being unpatentable over Fandrianto, Duncan or Thi in view of Lim and in further view of Nguyen. The Examiner's rejections are respectfully traversed.

Applicant has demonstrated that independent claim 11 is allowable. Because claims 22-25 depend from claim 11, applicant respectfully submits that these claims are also allowable. Applicant has demonstrated that independent claim 1 is allowable. Because claims 4-6 depend from claim 1, applicant respectfully submits that these claims are also allowable. Independent claim 26 includes at least limitations that are similar to the limitations of claims 1 and 11. Accordingly, applicant respectfully submits that claim 26 is allowable. Because claims 27 and 31-34 depend from claim 26, applicant respectfully submits that these claims are also allowable. Applicant respectfully requests that the rejections of claims 4-6, 22-27 and 31-34 under 35 U.S.C. § 103(a) be withdrawn.

IV. Conclusion

For the reasons set forth above, this application is in condition for allowance. Entry of the amendments and a favorable action are respectfully requested.

Respectfully submitted,



Hassan Albakri
(Limited Recognition)
Agent for Applicant
FISH & NEAVE LLP
Customer No. 36981
1251 Avenue of the Americas
New York, New York 10020-1105
Tel.: (212) 596-9000
Fax : (212) 596-9090